US-PAT-NO: 6525609

DOCUMENT-IDENTIFIER: US 6525609 B1

TITLE: Large gain range, high linearity, low noise MOS VGA

---------- KWIC ---------

Brief Summary Text - BSTX (2):
Radio receivers, or tuners, are widely used in applications requiring the reception of electromagnetic energy. Applications can include broadcast receivers such as radio and television, set top boxes for cable television, receivers in local area networks, test and measurement equipment, radar receivers, air traffic control receivers, and microwave communication links among others. Transmission of the electromagnetic energy may be over a transmission line or by electromagnetic radio waves.

Drawing Description Text - DRTX (60):
FIGS. 44a and 44b are illustrations of an embodiment of comparator circuitry
used to activate individual LNA amplifier stages;

Detailed Description Text - DETX (18):
This type of resonant circuit used as a preselector will increase frequency
selectivity of a receiver that has been designed with this stage at its input.
If an active preselector circuit is used between an antenna and frequency
conversion stages, the sensitivity of the receiver will be increased as well as
improving selectivity. If a signal is weak its level will be close to a
background noise level that is present on an antenna in addition to a signal.

It this signal cannot be separated from the noise, the radio signal will not be
able to be converted to a signal usable by the receiver. Within the receiver's
signal processing chain, the signal's amplitude is decreased by losses at every
stage of the processing. To make up for this loss the signal can be amplified
initially before it is processed. Thus, it can be seen why it is desirable to
provide a circuit in the receiver that provides frequency selectivity and

	Document ID	Kind Codes	Source	Issue Date	Pages	
34	US 6525609 B1		USPAT	20030225	123	Large
35	US 6509796 B2		USPAT	20030121	170	Varia
36	US 6500715 B2		USPAT	20021231	62	Metho
37	US 6466634 B1		USPAT	20021015	58	Radio
38	US 6445039 B1		USPAT	20020903	100	Syste
39	US 6426680 B1		USPAT	20020730	151	Syste
40	US 6304648 B1		USPAT	20020917	3333	Radio
41	US 6351190 B1		USPAT	20020226	3343	Stage

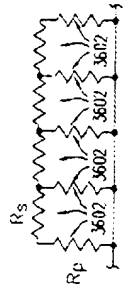


FIG. 39

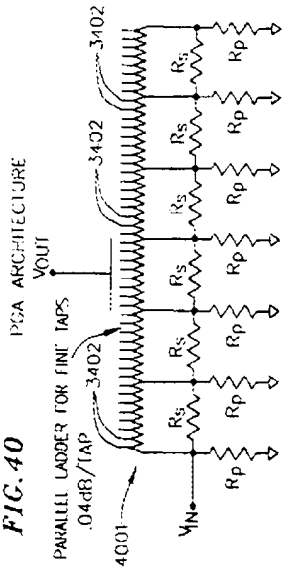


FIG. 40

FAST Browser - Tagged | JP 05249920 A | Tag S.P.T.I | Doc 9/11 | "Full" 4/6 (Total images 6) | Marked
File Edit View Tools Window Help
Courier New 12

CONSTITUTION: A gradation control driver 3 by means of pulse width
modulation and a scanning driver 4 are connected to a matrix
display panel 10
composed of plural number of electrodes. A control circuit 1
addresses to a
ROM 2, and reads gradation clocks in a single horizontal
period, and transmits
them to the gradation driver 3. At this time, which clocks
in the ROM are
adopted is determined according to respective display
devices. The
control circuit 1 counts the gradation clocks corresponding
to display data of
respective picture elements, and determines a corresponding
pulse width, and
addresses pulses on the picture elements, and
control is carried out
by changing the magnitude of effective voltage applied to
liquid crystal. In
this case, to put it concretely, the ROM 2 writes clock data
in the ROM having
a byte length of four bits, and selection of bits is carried
out by means of
jumper wires.

Document Identifier - DID (1):

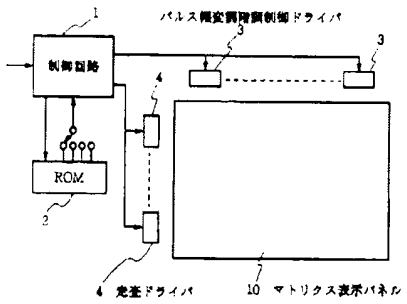
Current US Cross Reference Classification - CCXR (1):

Details Text Image HTML FWC

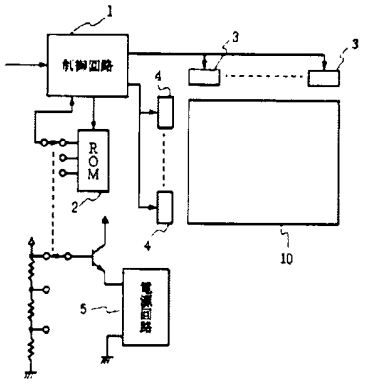
	U	1	Document ID	Issue Dat	Pages	Ti
8	☐	☑	JP 02253170 A	19901011	1	LIQUID CRYSTAL DRIVER CHE
	☐	☑	JP 05249920 A	19930928	6	DRIVING CIRCUIT FOR LIQUI
10	☐	☑	JP 05173503 A	19930713	12	DATA DRIVER CIRCUIT FOR L DEVICE
11	☐	☑	JP 04102892 A	19920403	11	DRIVING CONTROL SYSTEM FO DEVICE

Details Text Image HTML

【図1】



【図2】



Details Text Image HTML Full

PLAST Browser - Tagged | JP 05173503 A | Tag S.P.11 | Doc 10/11 | "Full" 11/12 (Total images 12) | Marked
File Edit View Tools Window Help

CONSTITUTION: In the data [illegible] circuit 30 of a [illegible] display
device 26 provided with a first and a second latches 22, 23
having the capacity
corresponding by one display row of the image data of an
interlace system and
transferring the image data from the first latch 22 to the
second latch 23
after fetching the image data by one display row into the
first latch 22 and
selecting a [illegible]
of the output of
the second latch 23 and applying it to a [illegible]
cell, a [illegible]
[illegible] replacing means 25 reading twice the holding content
of the second
latch 23 and providing a polarity inverting means 24
inverting the polarity of
the reading data of one side and further replacing the order
of the [illegible]
[illegible] data of one side and further replacing the order of
the [illegible]
[illegible] corresponding to the reading data of one side is
provided.

Document Identifier - DID (1):

[illegible]

Title of Patent Publication - TTL (1):

DATA [illegible] CIRCUIT FOR [illegible] DISPLAY DEVICE

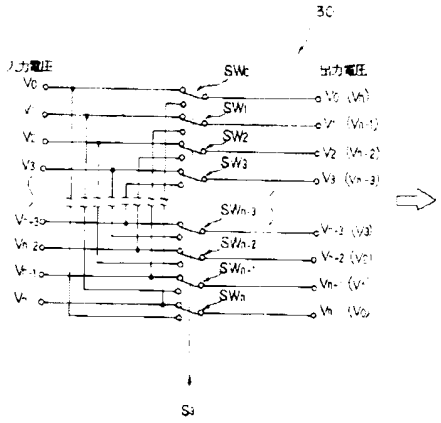
Details | Text | Image | HTML | WIC

	U	1	Document ID	Issue Dat	Pages	Ti
7	☐	☑	US 5892494 A	19990406	19	Correction of LCD drive v LCD switching element tur
8	☐	☑	JP 02253170 A	19901011	1	LIQUID CRYSTAL DRIVER CHE
9	☐	☑	JP 05249920 A	19930928	6	DRIVING CIRCUIT FOR LIQUI
10	☐	☑	JP 05173503 A	19930713	11	DATA DRIVER CIRCUIT FOR L DEVICE

Details | Text | Image | HTML

【図7】

第2実施例の階調電圧反転回路の構成図



Details | Text | Image | HTML | Full

[LAST Browser - L21 (17) 19 AND (345/ [JP 05173503 A | Tag S | Doc 9/17 | "Full" 11/12 (Total images 12)

File Edit View Tools Window Help

Courier New 12

PAT NO: JP405173503A

DOCUMENT-IDENTIFIER: JP 05173503 A

TITLE: DATA [illegible] CIRCUIT FOR [illegible] DISPLAY DEVICE

--------- KWIC ---------

Abstract Text - FPAR (2):

CONSTITUTION: In the data [illegible] circuit 20 of a [illegible] display device 26 provided with a first and a second latches 22, 23 having the capacity corresponding by one display row of the image data of an interlace system and transferring the image data from the first latch 22 to the second latch 23 after fetching the image data by one display row into the first latch 22 and selecting a [illegible] the output of the second latch 23 and applying it to a [illegible], a [illegible] replacing means 25 reading twice the holding content of the second latch 23 and providing a polarity inverting means 24 inverting the polarity of the reading data of one side and further replacing the order of the [illegible] data of one side and further replacing the order of the [illegible] corresponding to the reading data of one side is provided.

Details Text Image HTML KWIC

	U	1	Document ID	Issue Dat	Pages	Ti
6		☑	JP 05249920 A	19930928	6	DRIVING CIRCUIT FOR LIQUI
7			JP 05224626 A	19930903	7	LIQUID CRYSTAL DISPLAY DE
8			JP 05203918 A	19930813	5	ACTIVE MATRIX LIQUID CRYS
[illegible]			JP 05173503 A	19930713	12	DATA DRIVER CIRCUIT FOR L DEVICE
10	☑		JP 05119744 A	19930518		LIQUID CRYSTAL DISPLAY DE

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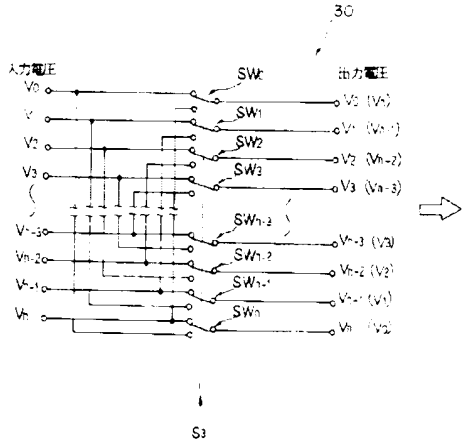
(図7)

第2実施例の階調電圧反転回路の構成図



Details Text Image HTML Full

EAST Browser - L20 (1) 19 AND (324/ | JP 02253170 | Tag S.P.11 | Doc 1/1 | "Clipped" 1/1 (Total images 1) | Marked

File Edit View Tools Window Help

Courier New 12

---------- KWIC ----------

Abstract Text - FPAR (2):

CONSTITUTION: First and second differential amplifiers 2 and 3 activate an AND gate 4 when an output signal 1 of the LCD driver is between an upper limit set voltage 8 and a lower limit set voltage 9 generated by D/A converters 11 and 12. An AND gate 5 acts to permit the input of a clock 6 to a clock counting circuit 7 only when the output of the gate 4 is in the active state. A GPU 10 reads the output value of the counting circuit 7 to detect the time of the signal of the LCD driver output stage outputted between the upper limit set voltage 8 and the lower limit set voltage 9. Thus, [illegible] processing functions (the output [illegible] and the time of the occurrence of the output [illegible]) of the LCD driver are simultaneously measured.

Title of Patent Publication - TTL (1):

[illegible] CHECKING CIRCUIT

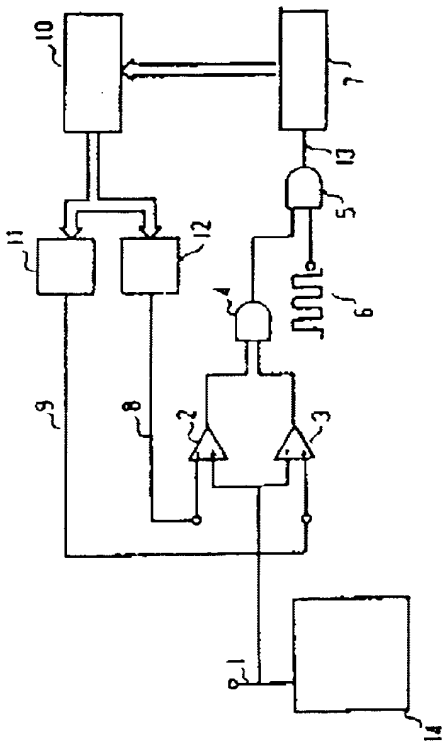
Current US Cross Reference Classification - CCXR (1):

[illegible]

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
	JP 02253170 A		JPO	19901011	1	LIQUI

Details Text Image HTML



Details Text Image HTML Clipped

EAST Browser - L1 (17) ((liquid wit | US 20020126076 | Tag S | Doc 3/17 | "Full" 16/50 (Total images 50)
File Edit View Tools Window Help
Courier New 12

DOCUMENT-IDENTIFIER: US 20020126076 A1

TITLE: Liquid crystal display device and method of driving the same

-------- - KWIC ---------

Claims Text - CLTX ...:

1. A liquid crystal display device comprising: (a) a first substrate; (b) a second substrate; (c) a liquid crystal layer sandwiched between said first and second substrates; (d) a plurality of scanning lines arranged on said first substrate; (e) a plurality of signal lines arranged on said first substrate; (f) a plurality of first switches arranged at intersections of said scanning lines and said signal lines; (g) a plurality of pixel electrodes each electrically connected to each of said first switches; (h) a plurality of opposing electrodes each arranged in parallel with each of said pixel electrodes; and (i) a signal line driver which switches a first ... for driving a positive pole and a second ... for driving a negative pole at a ... determined interval in accordance with a ... and outputs said positive or negative driving ... to said signal lines, said signal line driver compensating for said first and second ... such ...

Details Text Image HTML KWIC

	U	1	Document ID	Issue Dat	Pages	Ti
	☐	☐	US 20020126076	20020912	50	Liquid crystal display de the same
4	☐	☑	US 20020109656	20020815	10	Liquid crystal display de thereof
5	☐	☐	US 20020075272	20020620	22	Display control device an apparatus
6	☐	☐	US 20020050972	20020502	16	Dot-inversion data driver display device
7	☐	☐	US	20020307	11	Shift register and drivin

Details Text Image HTML

FIG. 18

GRADATION	REFERENCE	POSITIVE POLE	NEGATIVE POLE	AVERAGE	GRADATION COMPENSATION
255	REFERENCE 1	11.00V	0.60V	5.8V	–
234	REFERENCE 2	9.97V	1.63V	5.8V	–
240	REFERENCE 3	9.41V	2.19V	5.8V	–
192	REFERENCE 4	8.66V	2.94V	5.8V	–
128	REFERENCE 5	7.93V	3.67V	5.8V	–
84	REFERENCE 6	7.05V	4.55V	5.8V	–
32	REFERENCE 7	6.30V	5.30V	5.8V	–
0	REFERENCE 8	5.80V	5.80V	5.8V	–

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